multiLane

DATASHEET

Innovation for the next generation

ML4039B

4-Lane | 200G BERT | 1.25 – 29 GBd | NRZ & PAM4

4 Differential Error Detectors with CDR | 4 Differential Pulse Pattern Generators | PRBS31Q, SSPRQ & Custom Pattern | Adaptive FFE on receivers | Pre and Post Emphasis on TX | Real FEC analysis

Summary

With the accelerated growth of hyperscale datacenters, performance demands of Ethernet networks are increasing exponentially. As customer expectations for high-speed data throughput are at an all-time high, Bit Error Rate Testers (BERTs) have become a cornerstone for physical layer testing. Use cases range from qualifying bit transmission for fiber optic and copper-wire digital data transmission lines to testing signal integrity.

A BERT generates a sequence of bits through a communication channel and the received bits are then compared against the transmitted bits. A Bit Error Ratio (BER) quantifies the full end-to-end performance of a connectivity system and assures communication reliability. Additionally. This BERT supports the increasingly crucial real hardware FEC analysis to understand how your DUT will behave in a real data center environment.

The ML4039B is a 4-lane 200G BERT ideal for the testing of active semiconductor implementations. Some of its highlighted features include 4 differential error detectors and pulse pattern generators, custom pattern generation in addition to PRBS and SSPRQ, adaptive receiver FFE, transmitter pre/post-emphasis and progressive troubleshooting capabilities.

ML4039B

200G BERT

Introduction

The ML4039B is a fully featured 200G Bit Error Rate Tester. It has instrument-grade 2.92 mm coaxial connectors and covers a wide range of bitrates between 1.25 and 29 Gigabaud, while supporting both NRZ and PAM4 encoding schemes.

The GUI supports individual control of each TX level, equalization, eye balance, and pattern selection. The user may also inject error sequences into the stream. The receiver features CTLE and FFE equalization that, in combination with TX FFE, compensates for up to 30 dB of loss at Nyquist. It also enables advanced debug capabilities by showing separate LSB and MSB BER, offering targeted error-insertion and allowing real-time monitoring of the received signal histogram level, signal-to-noise ratio and receiver equalizer tap values.

The ML4039B supports real hardware FEC, with the following FEC modes:

Signal Mode	FEC Type	Speed	Link	Description
PAM4	RS544 KP4	4 x 53.125 Gbps	200G	4 FEC Links, each is 53 Gbps
PAM4	RS544 KP1	2 x 53.125 Gbps	100G	2 FEC Links, each is 100 Gbps, using all 4 channels
NRZ	RS528 KR1	4 x 25.78125 Gbps	100G	4 FEC Links, each is 25 Gbps

Key Features

- High-value, instrument-grade BERT optimized for high-speed data analysis of 100G/200G devices
- Wide range of bitrate coverage enables PHY testing for Ethernet, HDMI 2, USB 3.1, PCIe, Fiber-Channel and more
- Ability to tune the bit rate in very fine steps to facilitate finding the locking margin
- Supports PRBS13Q/15Q/31Q and user-defined patterns
- Low power consumption
- API library, sample code and Python wrapper

Typical Applications

- Production testing of modules, cables and optoelectrical ICs
- Benchtop testing for functional and SI validation
- Transceiver functionality validation testing

Using ThunderBERT GUI, both instant and accumulated BER measurements can be displayed and monitored:

Figure 1: ML4039B - ThunderBERT GUI Window

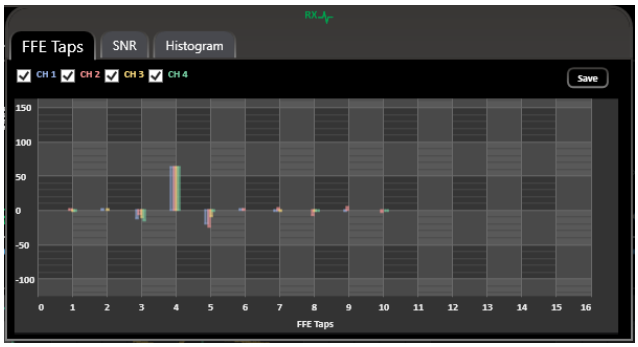

Figure 2: RX Diagnostics - FFE Taps using ML4039B

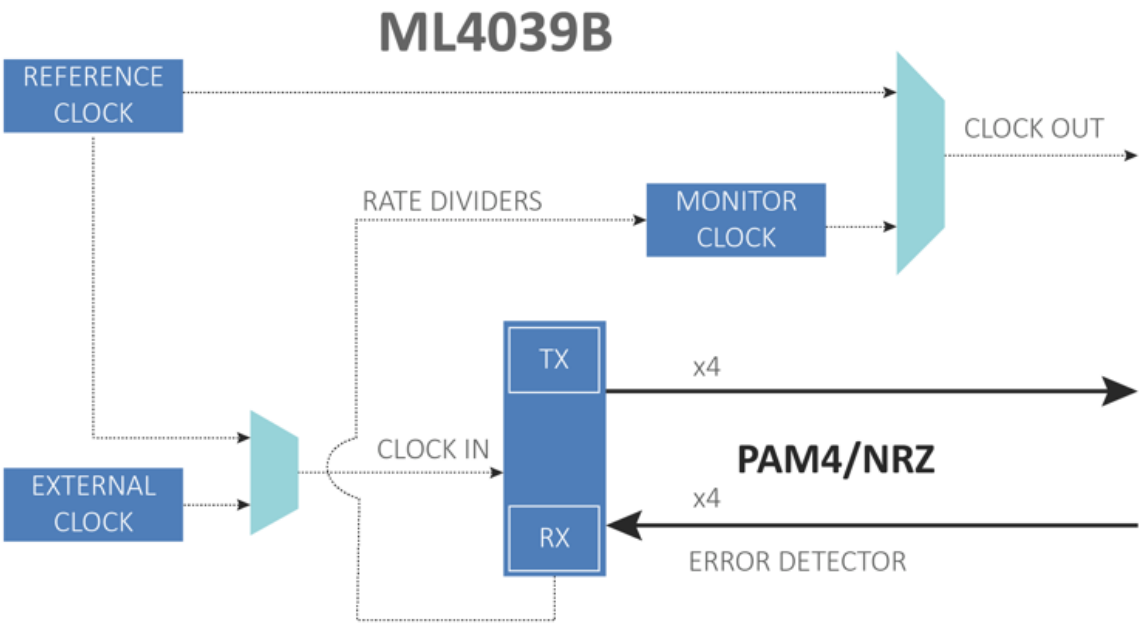

Figure 3: ML4039B Block Diagram

ThunderBERT GUI

The ThunderBERT GUI is highly intuitive and responsive, supporting a variety of tests and measurements on the ML4039B platform. Please refer to the ThunderBERT User's Guide for detailed operational instructions.

Figure 4: ML4039B front view

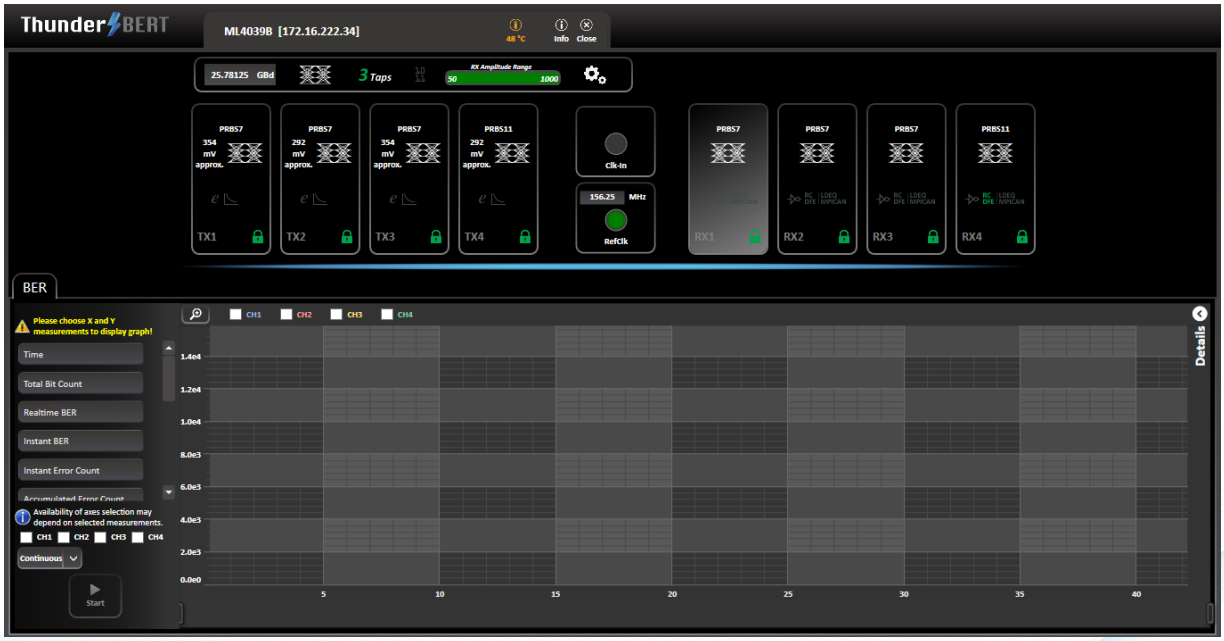

Figure 5: Main GUI

Electrical Specifications

Parameter		Specifications
Bit Rates		PAM4: 7 – 29 GBaud NRZ: 1.12 – 1.56 Gbps, 2.24 – 6.1 and 6.6 – 29 Gbps
TX Amplitude Differential		0 – 800 mVpp at 10 GBd 0 – 600 mVpp at 26 GBd
Patterns		PRBS 7/9/11/13Q/15/23/31Q/58/9_4 JP083B, IEEE 802.3bs, OIF-CEI-3.1 User defined
TX Amplitude Adjustment		Steps of 2 mV
Pre-Emphasis Resolution		±1000 steps
Equalizing Filter Spacing		1 UI
Random Jitter RMS		230 fs
Rise / Fall Time (20–80%)		15 / 15 ps
Error Detector sensitivity		50 mVpp
Input Equalizer Dynamic Range		Up to 30 dB
TX/RX connectors		2.92 mm
Clock	Reference	Up to 425 MHz, optimal value: 156.25 MHz
	Monitor	Up to 800 MHz, rate dividers: 4, 8, 16, 32, 64
	CDR[1]	Up to 800 MHz, rate dividers: 32, 64, 128, 256, 512, 1024, 2048, and 4096
Clock Input Range		80 - 700 MHz with an optimal value of 156.25 MHz
Clock Input Amplitude		200 - 1200 mV
Clock Input Impedance		50 Ω
Ambient Temperature		-15 to 40 °C
Weight		~1.5 kg
Dimensions LxWxH (cm)		35 x 22 x 9

1 - CDR Clock is available on the revision E of the ML4039B Hardware

Mechanical Dimensions

The ML4039B is a benchtop instrument which also fits in a 19-inch 2U rack. Two ML4039B arranged side by side take up a single 2-RU slot in a rack. MultiLane also supplies the needed brackets.

Ordering Information

Option	Description
ML4039B	200G BERT (4-lane up to 29 GBd)
3YW	Total 3-year warranty
CAL	Single calibration
3YWC	Total 3-year warranty with 3 annual calibrations
FEC	Real Hardware FEC

Recommended Accessories

Instruments	Recommended *Phase matched cable pairs*	Alternative *Phase matched cable sets*	Comments
ML4039B	8x MLCBPM-2.92-30	2x MLCBPM-2.92-30-8	2.92 mm connector 2x8 channel 30 cm
ML4039B	8x MLCBPM-2.92-60	2x MLCBPM-2.92-60-8	2.92 mm connector 2x8 channel 60 cm

Please contact us at sales@multilaneinc.com.